Features

• 200pin, Small-Outline Dual In-line Memory Module (SODIMM)
• Fast data transfer rates: PC2-4200, PC3-5300, PC3-6400
• Single or Dual rank
• 512MB (64Meg x 64), 1GB(128 Meg x 64), 2GB (256 Meg x 64)
• JEDEC standard 1.8V I/O (SSTL_18-compatible)
• $V_{DD} = V_{DDQ} = 1.8V \pm 0.1V$
• $V_{DDSPD} = 3.0V$ to 3.6V
• Differential clock inputs, Differential data strobe (DQS, DQS#) option
• 4*n*-bit prefetch architecture
• Multiple internal device banks for concurrent operation
• Programmable CAS latency (CL)
• Posted CAS additive latency (AL)
• WRITE latency = READ latency - 1 tCK
• Programmable burst lengths (BL): 4 or 8
• Adjustable data-output drive strength
• 64ms, 8,192-cycle refresh
• On-die termination (ODT)• Serial presence-detect (SPD) EEPROM
• Gold edge contacts
• Pb-free

Module Specification

Part Number	Module Density & Configuration	Bandwidth	Data Rate	Timing (tCL-tRCD-tRP)
SP512MBSRU533O01(2)	512MB (64Mx64) 64Mx8 1Rank	PC2-4200	DDR2-533	4-4-4
SP512MBSRU667O01(2)		PC2-5300	DDR2-667	5-5-5
SP001GBSRU533Q01(2)	1GB (128Mx64) 64Mx16 2Ranks	PC2-4200	DDR2-533	4-4-4
SP001GBSRU667Q01(2)		PC2-5300	DDR2-667	5-5-5
SP001GBSRU800Q02		PC2-6400	DDR2-800	5-5-5
SP001GBSRU667O01(2)	1GB (128Mx64) 64Mx8 2Ranks	PC2-5300	DDR2-667	5-5-5
SP001GBSRU800O01		PC2-6400	DDR2-800	5-5-5
SP001GBSRU533S01(2)	1GB (256Mx64) 128Mx8 1Rank	PC2-4200	DDR2-533	4-4-4
SP001GBSRU667S01(2)		PC2-5300	DDR2-667	5-5-5
SP001GBSRU800S01(2)		PC2-6400	DDR2-800	5-5-5
SP002GBSRU533S01(2)	2GB (256Mx64) 128Mx8 2Ranks	PC2-4200	DDR2-533	4-4-4
SP002GBSRU667S01(2)		PC2-5300	DDR2-667	5-5-5
SP002GBSRU800S01(2)		PC2-6400	DDR2-800	5-5-5

Note:

1. This document supports all SRU Series DDR2 200Pin SODIMM products.
2. Some item was being EOL in this list, Please contact with our sales Dep.
3. All part numbers end with a double-digit code is for customize use only.
   Example: SP512MBSRU533O02-XX

Pin Assignments

200-Pin DDR2 SODIMM Front							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VREF	51	DQS2	101	A1	151	DQ42
3	VSS	53	VSS	103	VDD	153	DQ43
5	DQ0	55	DQ18	105	A10	155	VSS
7	DQ1	57	DQ19	107	BA0	157	DQ48
9	VSS	59	VSS	109	WE#	159	DQ49
11	DQS0#	61	DQ24	111	VDD	161	VSS
13	DQS0	63	DQ25	113	CAS#	163	NC
15	VSS	65	VSS	115	S1#	165	VSS
17	DQ2	67	DM3	117	VDD	167	DQS6#
19	DQ3	69	NC	119	ODT1	169	DQS6
21	VSS	71	VSS	121	VSS	171	VSS
23	DQ8	73	DQ26	123	DQ32	173	DQ50
25	DQ9	75	DQ27	125	DQ33	175	DQ51
27	VSS	77	VSS	127	VSS	177	VSS
29	DQS1#	79	CKE0	129	DQS4#	179	DQ56
31	DQS1	81	VDD	131	DQS4	181	DQ57
33	VSS	83	NC	133	VSS	183	VSS
35	DQ10	85	BA2	135	DQ34	185	DM7
37	DQ11	87	VDD	137	DQ35	187	VSS
39	VSS	89	A12	139	VSS	189	DQ58
41	VSS	91	A9	141	DQ40	191	DQ59
43	DQ16	93	A8	143	DQ41	193	VSS
45	DQ17	95	VDD	145	VSS	195	SDA
47	VSS	97	A5	147	DM5	197	SCL
49	DQS2#	99	A3	149	VSS	199	VDDSPD

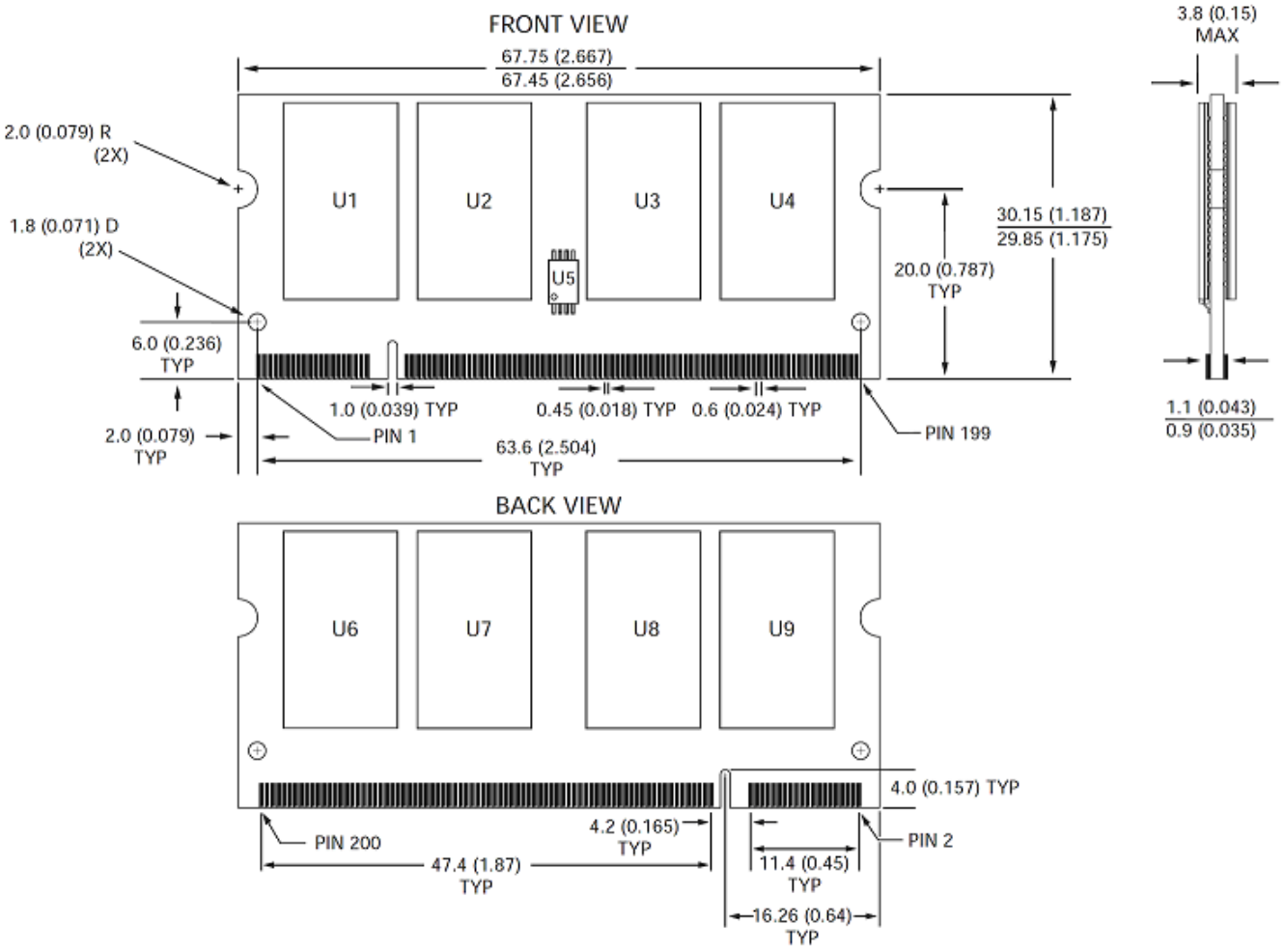
200-Pin DDR2 SODIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
2	VSS	52	DM2	102	A0	152	DQ46
4	DQ4	54	VSS	104	VDD	154	DQ47
6	DQ5	56	DQ22	106	BA1	156	VSS
8	VSS	58	DQ23	108	RAS#	158	DQ52
10	DM0	60	VSS	110	S0#	160	DQ53
12	VSS	62	DQ28	112	VDD	162	VSS
14	DQ6	64	DQ29	114	ODT0	164	CK1
16	DQ7	66	VSS	116	A13	166	CK1#
18	VSS	68	DQS3#	118	VDD	168	VSS
20	DQ12	70	DQS3	120	NC	170	DM6
22	DQ13	72	VSS	122	VSS	172	VSS
24	VSS	74	DQ30	124	DQ36	174	DQ54
26	DM1	76	DQ31	126	DQ37	176	DQ55
28	VSS	78	VSS	128	VSS	178	VSS
30	CK0	80	CKE1	130	DM4	180	DQ60
32	CK0#	82	VDD	132	VSS	182	DQ61
34	VSS	84	NC	134	DQ38	184	VSS
36	DQ14	86	NC	136	DQ39	186	DQS7#
38	DQ15	88	VDD	138	VSS	188	DQS7
40	VSS	90	A11	140	DQ44	190	VSS
42	VSS	92	A7	142	DQ45	192	DQ62
44	DQ20	94	A6	144	VSS	194	DQ63
46	DQ21	96	VDD	146	DQS5#	196	VSS
48	VSS	98	A4	148	DQS5	198	SA0
50	NC	100	A2	150	VSS	200	SA1

Pin Description

Symbol	Type	Description
A0–A13	Input (SSTL_18)	**Address inputs:** Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA0–BA2) or all device banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. A0–A12 (256MB) and A0–A13 (512MB, 1GB).
BA0–BA2	Input (SSTL_18)	**Bank address inputs:** BA0–BA2 define to which device bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0–BA2 define which mode register, including MR, EMR, EMR(2), and EMR(3), is loaded during the LOAD MODE command. BA0, BA1 (256MB, 512MB) and BA0–BA2 (1GB).
CK0, CK0#, CK1, CK1#, CK2, CK2#	Input (SSTL_18)	**Clock:** CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data (DQs and DQS/DQS#) is referenced to the crossings of CK and CK#.
CKE0 ,CKE1	Input (SSTL_18)	**Clock enable:** CKE (registered HIGH) activates and CKE (registered LOW) deactivates clocking circuitry on the DDR2 SDRAM.
ODT0, ODT1	Input (SSTL_18)	**On-die termination:** ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to the following pins: DQ, DQS, DQS#, and CB. The ODT input will be ignored if disabled via the LOAD MODE command.
RAS#, CAS#, WE#	Input (SSTL_18)	**Command inputs:** RAS#, CAS#, and WE# (along with S#) define the command being entered.
S0#, S1#	Input (SSTL_18)	**Chip select:** S# enables (registered LOW) and disables (registered HIGH) the command decoder.
SA0–SA2	Input (SSTL_18)	**Presence-detect address inputs:** These pins are used to configure the presence-detect devices.
SCL	Input (SSTL_18)	**Serial clock for presence-detect:** SCL is used to synchronize the presence-detect data transfer to and from the module.
SDA	I/O	**Serial presence-detect data:** SDA is a bidirectional pin used to transfer addresses and data into and out of the presence-detect portion of the module.
DM0–DM7	I/O (SSTL_18)	**Data input mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with that input data, during a write access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading is designed to match that of DQ and DQS pins.
DQ0–DQ63	I/O (SSTL_18)	**Data input/output:** Bidirectional data bus.
DQS0–DQS7, DQS0#–DQS7#	I/O (SSTL_18)	**Data strobe:** Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. DQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
V_{DD}/V_{DDQ}	Supply	**Power supply:** 1.8V ±0.1V.
V_{DDSPD}	Supply	**Serial EEPROM positive power supply:** +1.7V to +3.6V.
V_{REF}	Supply	SSTL_18 reference voltage. ($V_{DD}/2$)
V_{SS}	Supply	Ground.
NC	–	**No connect:** These pins are not connected on the module.

Simplified Mechanical Drawing(x8 1Rank)

X64 DIMM, populated as one physical rank of x8 DDR2 SDRAMs

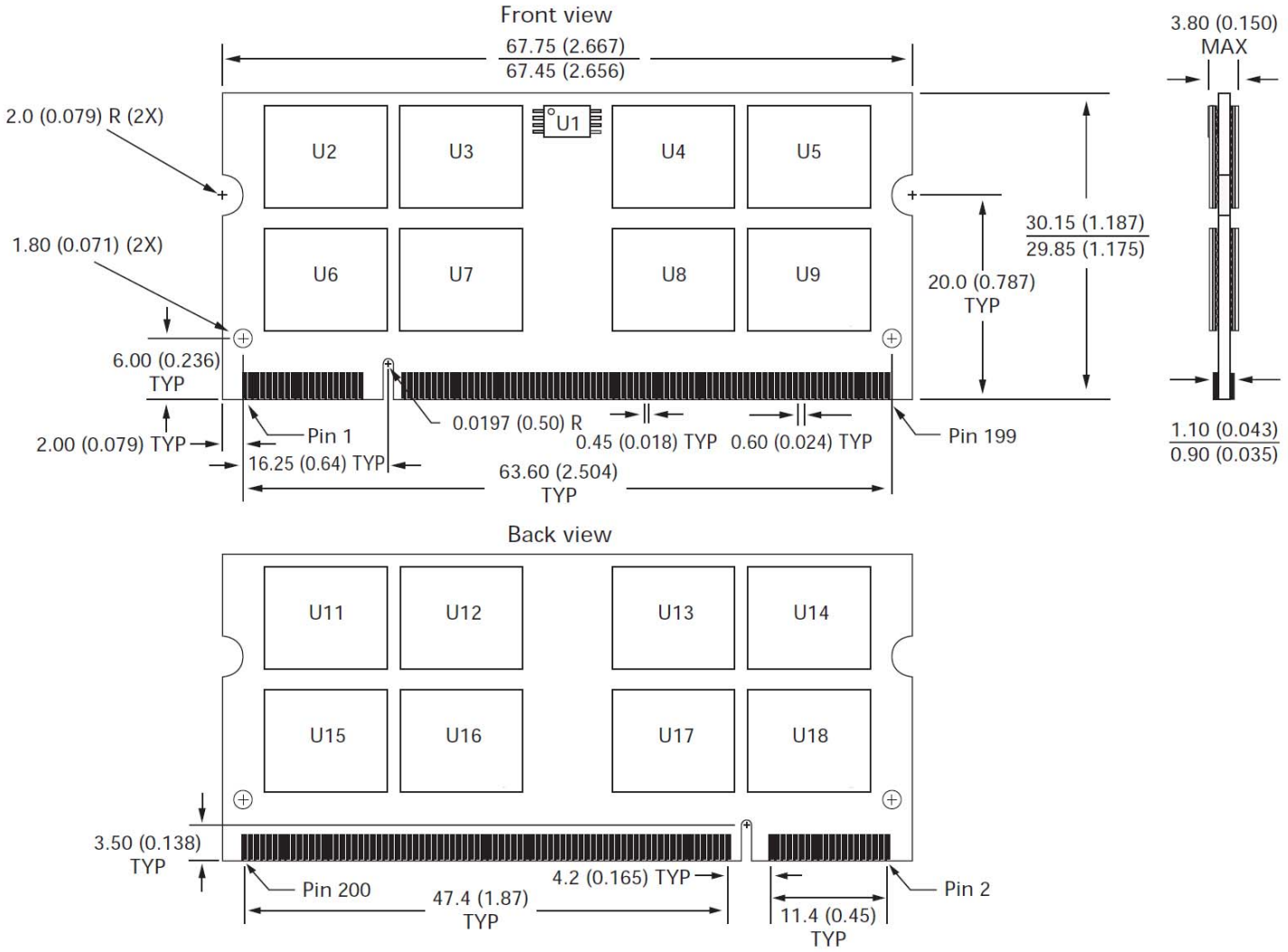


Note: 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.

Note: 2. The dimensional diagram is for reference only.

Simplified Mechanical Drawing(x8 2Ranks)

X64 DIMM, populated as one physical rank of x8 DDR2 SDRAMs

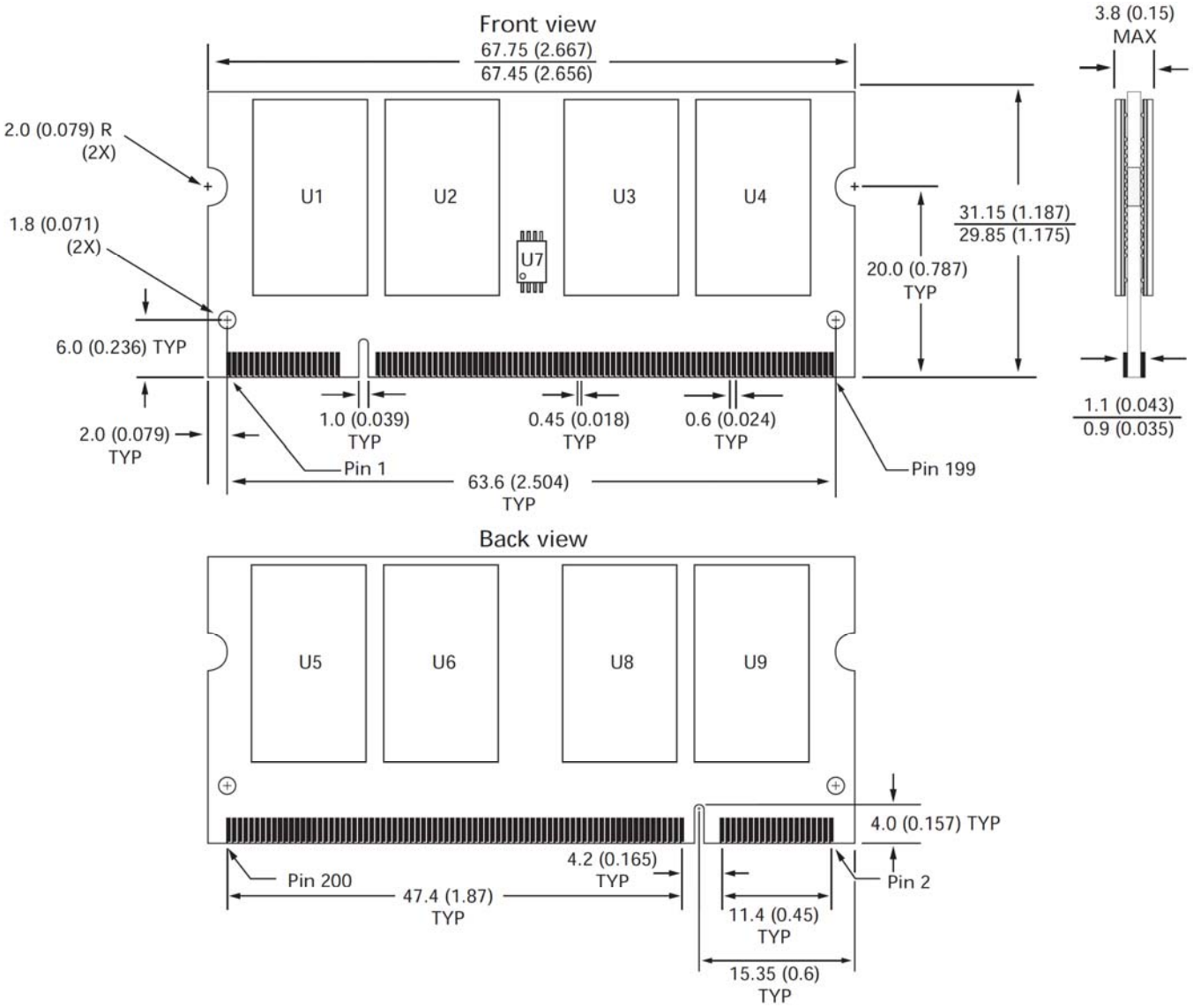


Note: 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.

Note: 2. The dimensional diagram is for reference only.

Simplified Mechanical Drawing(x16 2Ranks)

X64 DIMM, populated as one physical rank of x6 DDR2 SDRAMs



Note: 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.

Note: 2. The dimensional diagram is for reference only.